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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/605,293	CHAPEK, DAVID L.
	Examiner	Art Unit
	N. Drew Richards	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 6/1/04, PROSECUTION IS HEREBY REOPENED. The rejection of claim 9 has been altered to include a positive recitation of the silicon dioxide layer being formed on a semiconductor substrate. Also, new evidence in support of the obviousness of claim 12 is set forth below. It is noted that the evidence presented is merely provided as directly corresponding evidence in support of the Official Notice taken in the previous Office Actions. See MPEP 2144.03 (D).

To avoid abandonment of the application, applicant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

> be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art with Henley et al. (U.S. Patent No. 6083324).

With regard to claim 9, Burns et al. teach in figure 9.8 on page 381 a semiconductor substrate, a silicon dioxide layer formed on the substrate, and a layer of polycrystalline silicon formed on the layer of silicon dioxide. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein and being free of sputtered metal contaminants or the layer of polycrystalline silicon having a smooth morphology.

Applicant's admitted prior art discloses on page 1 lines 5-22 a layer of silicon dioxide having been doped with hydrogen ions so that a layer of polycrystalline silicon formed thereon will have a smooth morphology. The admitted prior art does not teach the layer of silicon dioxide being free of sputtered metal contaminants as the Kaufman ion source causes metal contaminants in the layer. The admitted prior art teaches the metal contaminants being produced from metal sputtering off a metal grid in the Kaufman ion source apparatus and that as device sizes decrease the effect of the damage from the metal contaminants increases.

Henley et al. teach a plasma immersion ion implantation apparatus for implanting hydrogen ions into semiconductors. It is noted that plasma source ion

implantation (PSII or PSI) and plasma immersion ion implantation (PIII) are interchangeable terms for the same plasma treatment. Henley et al. teach that their implantation method can be used on SOI (silicon-on-insulator) substrates in column 2 lines 30-40 and teach implanting hydrogen ions in line 38, for example.

Applicants admitted prior art and Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant the hydrogen using the PSII technique of Henley et al. The motivation for doing so is to that PIII is cost effective, easy to use, and produces less impurity metal contamination. Therefore, it would have been obvious to combine Applicant's admitted prior art with Henley et al. to alleviate the metal contamination.

Burns et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 9. In the combination of the references, the layer of polycrystalline silicon formed on the layer of silicon dioxide would have a smooth morphology.

With regard to claim 10, Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, a silicon dioxide layer formed on at least a portion of the substrate, a layer of polycrystalline silicon formed on at least a portion of the silicon dioxide layer, and a gate oxide formed on the substrate from the layer of silicon dioxide, and a source and a drain in the substrate where a gate electrode is formed on the substrate from the layer of polycrystalline silicon. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16 and Henley et al. teach using a PSII method to implant the hydrogen. Applicant's admitted prior art with Henley et al. as discussed above also teach the silicon dioxide as being free of sputtered metal contaminants. In the combination of the references, the gate oxide would be formed from the layer of silicon dioxide having hydrogen ions implanted therein and the layer of polycrystalline silicon formed on the layer of silicon dioxide would have a smooth morphology.

Burns et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon

film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon. The gate oxide for each transistor of the combination of references would be formed of the silicon dioxide having hydrogen atoms implanted therein as taught above with regard to claim 10.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon. As evidence that is it well known in the art at the time of the invention that a wafer is divided into a plurality of die see Wolf et al. In figure 3, Wolf et al. shows an entire wafer processed (in the wafer

processing steps), probed, and then diced into ~50 to 1000 chips. Thus, Wolf et al. is direct evidence that it is obvious to split a wafer into a plurality of chips.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art with Henley et al. as applied to claims 9-12 above.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate 501 of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a gate oxide formed from the insulating layer, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Henley et al. as discussed above teach using a PSII method to implant the hydrogen. Applicant's admitted prior art with Henley et al. as discussed above also teach the silicon dioxide as being free of sputtered metal contaminants. In the combination of the references, the layer of polycrystalline silicon formed on the layer of substrate would have a smooth morphology.

Murata et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the

invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 14.

Response to Arguments

5. Applicant's arguments filed 6/1/04 have been fully considered but they are not persuasive. The arguments responded to below are those presented in applicant's Appeal Brief.

In applicant's "Summary of Argument" it is argued that no motivation exists to combine the teachings of "applicant's admitted prior art" with any of the cited references. This is not persuasive as proper motivation has been provided for combining the references in the rejection of each claim above. For example, the motivation from the rejection of claim 9 above for combining applicant's admitted prior art with Henley et al. is that PIII is cost effective, easy to use, and produces less impurity metal contamination. The motivation from the rejection of claims 10-12 above for combining Burns et al. with applicant's admitted prior art and Henley et al. is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. The motivation from the rejection of claim 14 above

for combining Murata et al. with applicant's admitted prior art and Henley et al. is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Thus motivation does exist to combine the teachings of the prior art as applied.

In applicant's "Summary of Argument" it is also argued that the examiner has used improper hindsight reconstruction in citing Henley et al. against the claims and ignored the fact that Henley et al. do not teach or suggest providing a surface treatment on a silicon dioxide substrate for the purpose of providing a subsequent layer of polycrystalline silicon which has a smooth morphology as claimed.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In the instant case, the knowledge relied upon for the rejection was within the level of ordinary skill in the art at the time the claimed invention was made. The suggestion of implanting hydrogen into silicon dioxide to provide a smoother polycrystalline silicon film (page 1 lines

12-15 of applicant's disclosure) and the motivation to reduce metal impurities (page 1 lines 20-22 of applicant's disclosure) is found in the cited references. It is noted that "applicant's admitted prior art" is treated as a prior art reference, and thus any information taught therein is considered knowledge within the level of ordinary skill at the time the invention was made and not knowledge gleaned only from the applicant's disclosure.

In response to applicant's argument that Henley et al. do not teach or suggest providing a surface treatment on a silicon dioxide substrate for the purpose of providing a subsequent layer of polycrystalline silicon which has a smooth morphology as claimed, Henley et al. was not relied upon for teaching this limitation. This was taught by applicant's admitted prior art. This argument attacks the Henley et al. reference individually without considering the combination of references used in the rejection. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further argues that the examiner's burden of establishing a prima facie case of obviousness has not been met. Applicant states that the proposed combination of references is not based on any objective teachings or suggestions in the references themselves, but rather is based on prohibited hindsight using the claimed invention as a blueprint. This is not persuasive as

the proposed combination of references is based upon objective teachings or suggestions in the references themselves. The admitted prior art teaches on page 1 lines 21-22 that metal contamination from an ion implantation apparatus is undesirable as the effect of the damage caused from the metal contamination increases as device size decreases. Henley et al. teach on column 3 lines 15-17 that PIII is cost effective, easy to use, and produces less impurity metal contamination than other ion implantation techniques. Thus, it would be obvious to use the implantation method of Henley et al. in the process of the admitted prior art to alleviate the metal contamination and this teaching comes from the references themselves and not from prohibited hindsight. Further, the admitted prior art provides objective teaching and suggestion for combining the teachings of the hydrogen implantation process into the Burns et al. and Murata et al. references. The admitted prior art teaches on page 1 lines 8-15 that implanting hydrogen into a layer of silicon dioxide allows for the deposition of a thinner and smoother polycrystalline silicon film which in turn allows smaller components to be formed using the thinner and smoother film. Thus it would have been obvious to implant hydrogen into a layer of silicon dioxide as taught by the admitted prior art in view of Henley et al. in the devices of Burns et al. and Murata et al. to allow for smaller devices and increased device integration and this teaching comes from the references themselves and not from prohibited hindsight.

Applicant argues that applicant's admitted prior art and Henley et al. are not properly combinable and do not provide any expectation of success.

Applicant argues that the teaching of Henley et al. alone that hydrogen may be implanted into semiconductor articles by a PSII method does not provide proper motivation for the examiner's proposed substitution. Though this teaching alone may not provide proper motivation, the references as a whole do provide proper motivation for the proposed substitution. The admitted prior art recognize the undesirability of metal contamination and Henley et al. state that their implantation method produces less impurity metal contamination. Thus, one of ordinary skill in the art would be motivated by the admitted prior art to reduce metal contamination during implantation of hydrogen and Henley et al. provides a substitute implantation method which can be used to implant hydrogen that results in reduced metal contamination. This motivation as taught by the references as a whole constitutes a proper motivation for the examiner's proposed substitution.

Applicant further argues that Henley et al. do not address the problem, and provide no expectation of a successful solution of that problem. Though the applicant does not state exactly what "problem" Henley et al. allegedly does not address or provide expectation of a successful solution to, it is assumed that the "problem" is the same as discussed in applicant's admitted prior art and in applicant's invention. Specifically, the problem is assumed to be reducing or eliminating sputtered metal contaminants from the implanted target. This is not persuasive as the references as a whole teach the undesirability of metal contamination. Specifically, the admitted prior art teaches the undesirability of

metal contamination and specifically teaches the metal contamination resulting from the Kaufman ion source. Henley et al. also discuss problems resulting from metal contamination such as degraded device characteristics including leakage current and oxide breakdown voltage (Henley et al. column 1 line 65 through column 2 line 8). Henley et al. then specifically states that the implantation method they use is an "improved processing technique" that "produces less impurity metal contamination than other ion implantation techniques" (Henley et al. column 3 ljnes 14-17) and thus solves the problem of the admitted prior art by reducing the metal contamination.

Applicant further argues that there is no motivation to combine the teachings as proposed by the examiner as Henley et al. do no teach or suggest implanting hydrogen ions on the surface of a layer of silicon dioxide which is formed on a semiconductor substrate as claimed. First, it is noted that none of the claims recite implanting hydrogen on the **surface** of a layer of silicon dioxide, the claims merely state a layer of silicon dioxide having been doped with hydrogen. The language of the claims does not limit the doping (implantation) to the surface. In response to this argument, the examiner again notes that Henley et al. is not relied upon to teach specifically implanting hydrogen on the surface of a layer of silicon dioxide which is formed on a semiconductor substrate. The admitted prior art is relied upon for teaching implanting hydrogen into silicon dioxide which is formed on a semiconductor substrate. Henley et al. is relied upon to teach an implantation method for implanting hydrogen that does not

produce the metal impurity contamination of the admitted prior art implantation method (Kaufman source). Applicant then argues that the examiner cannot choose to ignore the fact that Henley et al. do not teach a surface treatment, do not address the same problem, and provide no expectation of successful solution of that problem. In response, Henley et al. do not need to teach a surface treatment as the claims do not require a surface treatment. Henley et al. does address the same problem of metal impurity contamination, and Henley et al. explicitly states that the implantation method they employ produces less impurity metal contamination thus providing a reasonable expectation of success.

Applicant further argues that Henley et al. do not teach or suggest providing a layer of polycrystalline silicon on the doped layer of silicon dioxide which has a smooth morphology as claimed and that while the examiner has taken the position that this limitation is taught by applicant's admitted prior art, this teaching alone does not provide sufficient motivation to combine the teachings of the references. This is not persuasive as this teaching alone does not need to provide the motivation, the motivation can properly come from the teachings of the references as a whole. The examiner has explicitly pointed out numerous times proper motivation for combining the references that comes from the references themselves. Specifically, the examiner has explained how the motivation to combine the references comes from the admitted prior art and Henley et al.'s recognition of problems associated with metal impurity contamination and Henley et al.'s explicit statement that the implantation

technique they employ produces less impurity contamination than other ion implantation techniques.

Applicant further argues that one skilled in the art would not look to Henley et al. to correct the deficiencies of applicant's admitted prior art because Henley et al. do not teach implanting hydrogen ions on the surface of a silicon dioxide layer for the purpose of providing a smooth morphology for the subsequently deposited silicon layer. This is not persuasive as one of ordinary skill in the art when presented with the problem of metal impurity contamination from a specific ion implantation source (Kaufman source) would reasonably look to Henley et al. to correct this problem as Henley et al. explicitly states that the implantation technique they employ produces less impurity contamination than other ion implantation techniques. Henley et al. teach that hydrogen ions can be implanted using their technique and that doing so results in less impurity metal contamination. Thus, one of ordinary skill in the art would reasonably look to Henley et al. to correct the deficiencies of applicant's admitted prior art.

Applicant further argues that the desirability of the combination is not suggested in the prior art but is instead based on prohibited hindsight. This is not persuasive as the motivation (desirability) for the combination of the references does come from the prior art, not from applicant's disclosure of their own invention. As explained previously, applicant's admitted prior art is considered a prior art reference, and thus any information taught therein is considered

knowledge within the level of ordinary skill at the time the invention was made and not knowledge gleaned only from the applicant's disclosure.

Applicant further argues that there is nothing is Henley et al. which indicates that their implantation technique would be applicable to the surface of a silicon dioxide layer and would successfully result in a layer of silicon dioxide which is free of metal contaminants as claimed. First, the claims do not require implanting into the **surface** of a silicon dioxide layer. Second, Henley et al. does teach implanting hydrogen into semiconductor articles. One of ordinary skill in the art would recognize that, though not explicitly stated by Henley et al., the implantation method would reasonably be expected to operate when implanting into silicon dioxide. As far as the resultant layer being free of metal contaminants, the admitted prior art recognizes the specific source of the metal impurities (the metal grid in the Kaufman source (applicants disclosure page 1 lines 17-21) and the plasma source implantation of Henley et al. does not require the metal grid and is taught to produce less metal impurities. One of ordinary skill in the art would recognize that without the metal grid there would be no sputtered metal contaminants as claimed. Also, one of ordinary skill in the art would recognize that since Henley et al. uses the same implantation technique as the instant invention, it would have the same result of the implanted layer being "free of sputtered metal contaminants."

Applicant then argues that Henley et al. do not teach or suggest the use of hydrogen plasma ions to obtain a smooth morphology for a subsequently deposited polycrystalline silicon layer and that nothing in Henley et al. points directly to the use of hydrogen ions. This is not persuasive as the rejections do not rely upon Henley et al. for teaching these limitations as these limitations are taught by the admitted prior art.

Applicant further argues that Henley et al. does not address the problem solved by the present invention. Applicant points out that Henley et al. are concerned with removing impurities by forming gettering sites. While Henley et al.'s invention as a whole presents a device with gettering sites to remove impurities, Henley et al. do state that in addition to the benefits of gettering, their invention occurs by way of improved processing techniques using plasma ion implantation that produces less impurity contamination than other ion implantation techniques (Henley et al., column 3 lines 9-17). Thus, one of ordinary skill in the art would have looked to use the teachings of Henley et al. in conjunction with Applicant's admitted prior art in order to resolve the problem of implanting hydrogen ions into a target without sputtering metal impurities into the target.

Applicant argues with regards to claims 10-12 that there is no suggestion in Henley et al. to implant hydrogen ions on a layer of silicon dioxide in a semiconductor substrate, nor any suggestion that such would provide a smooth

morphology for a subsequently deposited layer of polycrystalline silicon. This argument has been treated extensively above and is still not deemed persuasive.

With regard to claim 10, applicant argues that there is no teaching or suggestion in Henley et al. to implant hydrogen ions on a layer of silicon dioxide in a semiconductor substrate, nor any suggestion that such would provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon on a silicon dioxide layer in a field effect transistor. This is not persuasive as clear and convincing motivation has been presented in the rejection of claim 10 to use the silicon dioxide layer of applicant's admitted prior art with Henley et al. in a field effect transistor such as that taught by Burns et al. The admitted prior art provides objective teaching and suggestion for combining the teachings of the hydrogen implantation process into the Burns et al. reference. The admitted prior art teaches on page 1 lines 8-15 that implanting hydrogen into a layer of silicon dioxide allows for the deposition of a thinner and smoother polycrystalline silicon film which in turn allows smaller components to be formed using the thinner and smoother film. Thus it would have been obvious to implant hydrogen into a layer of silicon dioxide as taught by the admitted prior art in view of Henley et al. in the devices of Burns et al. to allow for smaller devices and increased device integration.

With regard to claim 11, applicant argues that there is no teaching or suggestion in any of the references which would motivate one skilled in the art to

combine their teachings to make the claimed memory array, nor do the cited references provide any expectation of success. This is not persuasive as clear and convincing motivation has been presented in the rejection of claim 11 to use the silicon dioxide layer of applicant's admitted prior art with Henley et al. in a memory array such as that taught by Burns et al. The admitted prior art provides objective teaching and suggestion for combining the teachings of the hydrogen implantation process into the Burns et al. reference. The admitted prior art teaches on page 1 lines 8-15 that implanting hydrogen into a layer of silicon dioxide allows for the deposition of a thinner and smoother polycrystalline silicon film which in turn allows smaller components to be formed using the thinner and smoother film. Thus it would have been obvious to implant hydrogen into a layer of silicon dioxide as taught by the admitted prior art in view of Henley et al. in the devices of Burns et al. to allow for smaller devices and increased device integration. The references provide a reasonable expectation of success as they are from the same field of endeavor. One would reasonably expect that the implantation of hydrogen using the technique of Henley et al. would be successful for implanting into the silicon dioxide of the admitted prior art as Henley et al. teach successful implantation of hydrogen.

With regard to claim 12, the applicant argues that since the examiner has not provided a reference which teaches a semiconductor wafer which includes a plurality of die that the examiner has not established a prima facie case of obviousness. First, a prima facie case of obviousness has been met as each

limitation in the claim has been shown to have been obvious to one of ordinary skill in the art at the time of the invention. Second, it is noted that applicant has not presented any arguments against the Official Notice used or any arguments as to why the rejection is improper. Applicant has merely stated that no reference was supplied in support of the Official Notice. The issue at hand, forming the claimed transistor or memory array on a wafer including a plurality of die, is readily obvious to one of ordinary skill in the art. In response to this, the Examiner has provided a reference in support of the Official Notice. Wolf et al. has been supplied to show that a wafer is split into a plurality of die.

With regard to claim 14, applicant argues that there is no teaching or suggestion in Henley et al. to implant hydrogen ions on the surface of a semiconductor substrate, nor any expectation of success of obtaining a substrate which is free of metal contaminants and which provides a smooth morphology for a subsequently deposited polycrystalline silicon layer. These are the same arguments presented with regard to claims 9 and 10-12 and these arguments have been treated extensively above.

Further, applicant argues that Murata et al. do not address the problem solved by the claimed invention. This is not persuasive as Murata et al. do not need to address the same problem as the present invention to be used in a rejection of the claim. Murata et al. in view of the combination of applicant's admitted prior art and Henley et al. teach all the claimed limitations and thus

properly reject claim 14. Applicant lastly argues that nothing in the prior art references provides motivation for preparing the glass surface of the substrate of Murata et al. such that it is free of metal contaminants and such that the subsequent deposition of a polycrystalline silicon layer has a smooth morphology as claimed. This is not persuasive as applicant's admitted prior art combined with Henley et al. clearly teach motivation for growing a smoother polycrystalline silicon film to allow smaller components and increase device integration and clearly teach motivation for the substrate being free of metal contaminants to improve device performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800